Design and Fabrication of an 8-Qubit Multi-layer Surface-Electrode Ion Trap Quantum Processor Chip

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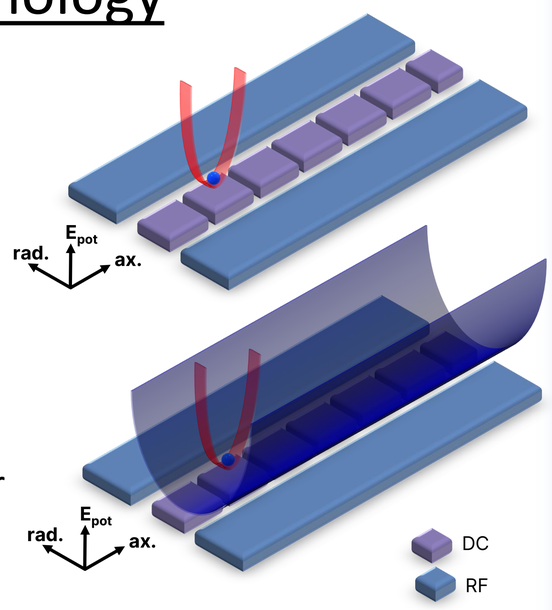
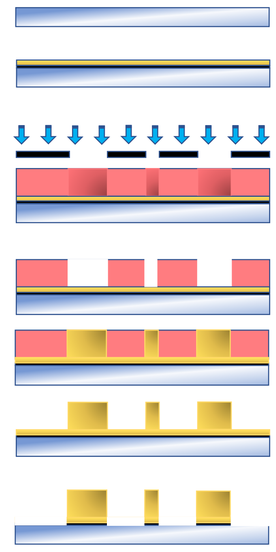
Ion Trap Technology

- A scalable platform for quantum information processing using trapped ions: **Surface-electrode Paul traps.**
- Ions are trapped above the surface by the fields emerging from the integrated RF and DC electrodes.
- Fast multi-ion qubit gates require higher motional frequency of ions, decreasing trap dimensions: Realized robustly by **Microfabrication** Techniques.[1]



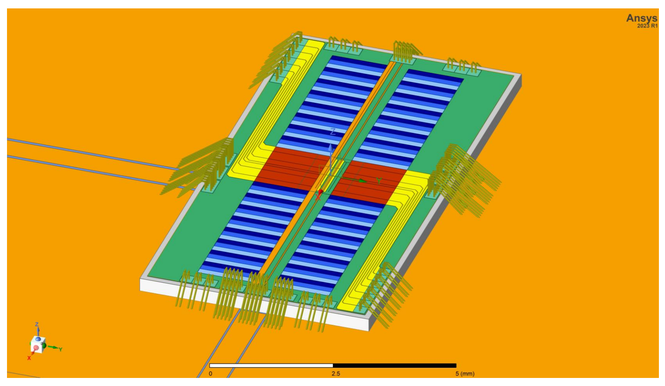
Microfabrication Process Single Layer

- Wafer cleaning.
- Evaporation of seed layer Ti/Au.
- UV-Photolithography: spin coating of photoresist, exposure and development.
- Electroplating and resist stripping.
- Reactive Ion Etching (RIE) to remove seed layer.



Demonstrator Chip Design

- 5 mm x 10 mm chip with two storage registers and a gate zone.
- Merging, splitting and swapping operations of ions.
- 2-qubit gates and all-to-all connectivity

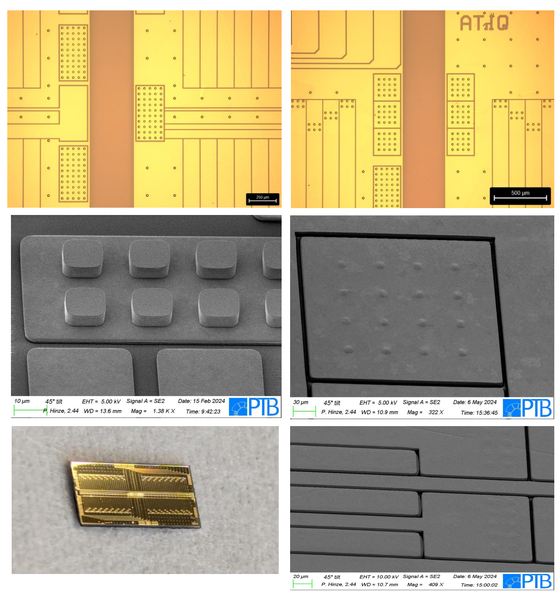


The multi core demonstrator design (HFSS Image)

- The buried first layer: microwave line and control electrodes.
- Metallized vias to the second layer with segmented DC electrodes and the radio frequency line.
- The embedded single microwave conductor as a bilayer meander is intrinsically amplitude and phase stable [4].

Demonstrator Chip Fabrication

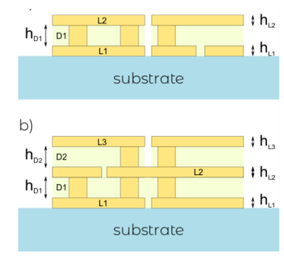
- UV-lithography with prior designed and produced photomask.
- Electrode fabrication using in house electroplating setup.
- Optical analysis to confirm target electrode heights and gap sizes.
- Iterative Lithography, RIE and CMP steps to free the via surface from Polyimide.



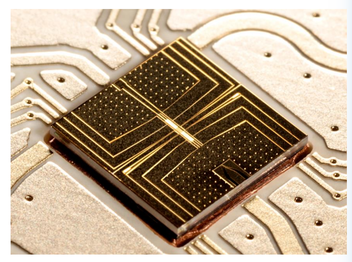
Optical/SEM images of the trap chip at various steps of the multilayer fabrication

Multilayer Traps [2]

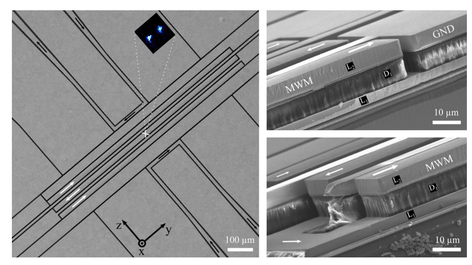
- Scalability with more metal layers.
- Flexibility through higher degree of freedom in signal routing.
- Metallized vias interconnecting layers
- Requires: polyimide coating, curing & Chemical Mechanical Polishing (CMP).



Multilayer Processing (MLP) [2]



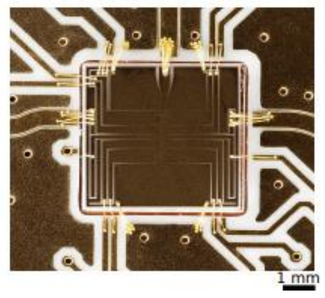
Fabricated Multilayer ion trap [3]



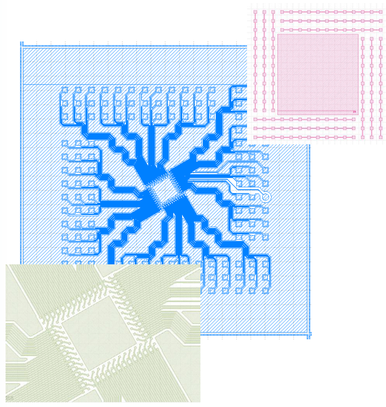
SEM image of the trap chip center fabricated using the MLP method [2]

Packaging: Flip-Chip Technology

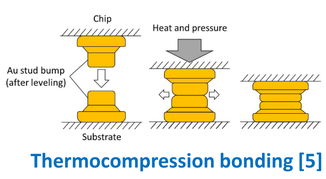
- Through substrate vias (TSVs) and connection with flip-chip technology as alternative for wire bonds. Implementation requires interposer technology.
- Thermocompression method to establish Au-Au bond [5]. Bonding requirements: 1N per bump and 200°C.



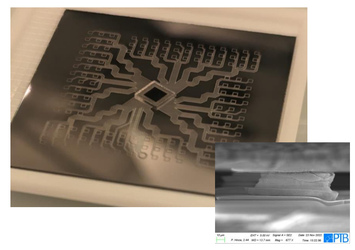
An ion trap with wire bonds



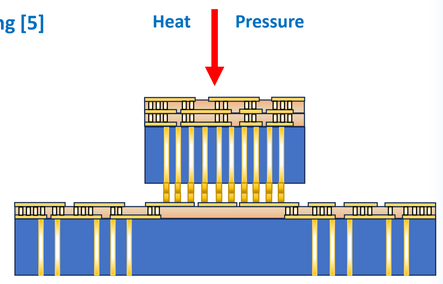
QVLS-Q1 Interposer and chipbackside layouts for Flip Chip tests



Thermocompression bonding [5]



Bonded test sample & SEM image of a bond (thermocompression: Au stud bump)



Schematic sketch of an assembly with interposer technology, TSVs and flip-chip bonding

Outlook

- Improving yield of microfabrication process for multilayer ion traps.
- Packaging of ion traps implementing flip-chip technology in the next version of the multicore demonstrator chip.
- Hybrid integration.

References

- [1] S. Seidelin et al., PRL 96, 253003 (2006)
- [2] A. Bautista-Salvador et al. New J. Phys. **21**, 043011 (2019) Patent DE 10 2018 111 220 (2019)
- [3] H. Hahn, G. Zarantonello et al., ArXiv 1812.02445
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